International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 3 Issue: 3 1129 - 1131

Design styles of Asymmetric nMOS and their Simulation

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***Abstract*—** Scaling down of the MOSFET has been done extensively to meet the need for high speed devices. Symmetric MOSFET with LDD structure could not mitigate the short channel effects, as the device was scaled down to deep sub-micrometer regime. Asymmetric MOSFET design styles were thus adopted to achieve increased device speed. In this paper, two asymmetric MOSFETs are designed and simulated using device simulator (SILVACO) - one with LDD at drain side only and second with unequal junction depths.

Keywords-*short channel effects, lightly doped drain (LDD), Si-SiO$_2$ interface, hot electron effects, impact ionization.*

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I. INTRODUCTION

With the evolution of high speed and portable devices, the MOSFET scaling down has been increased drastically which led to an increased package density [1] [2]. This continuous scaling down of the device leads to some serious problems such as increase in the electric fields in the channel or breakdown of the Si-SiO$_2$ interface. These are called short channel effects [3].

Since a symmetric MOSFET with gate length deep down to nanometer size could not prevent the device from short channel effects, asymmetric design styles were adopted. In this paper, two 50nm asymmetric MOSFETs are designed. One with LDD (lightly doped drain) [4] structure at drain only and other having unequal junction depths. These structures are designed and simulated using device simulator SILVACO in the nanometer regime. For designing of the asymmetric MOSFET, the p type bulk was doped with boron. Then oxide layer of thickness 2nm was deposited. As+ ions were implanted to form the LDD structure. Finally, for heavy source drain implant heavy dosage of As^+ ions were used. With proper contact patterning, the electrodes were formed.

II. ASSYMMETRIC MOSFET STRUCTURE WITH LDD AT DRAIN ONLY

An asymmetric MOSFET structure with LDD at drain only was designed with gate length of 50nm and oxide thickness of 2nm. Since there exists parasitic resistance in the LDD regions, in this asymmetric MOSFET, as there is no LDD at the source, parasitic resistance would comparatively be less and hence the on-current would increase [7].

For the design of the asymmetric MOSFET with LDD at drain only, the p type bulk was doped with boron dose 1 x 10^{14} cm^{-2}. Then oxide layer of thickness 2nm was deposited. B^+ ions of dosage 2 x 10^{13} were used for threshold voltage adjustment. After proper etching, As^+ ions dose 4.5 x 10^{12} cm^{-2} were implanted to form the LDD structure. For heavy source drain implant As^+ ions dose 1 x 10^{15} cm^{-2} were used. In order to remove LDD from the source side, first LDD oxide was deposited over the polysilicon then the spacer at the source was etched to diffuse the heavy source region directly as shown in fig. 1. Then electrodes were formed with proper etching and patterning and metal connections were made.

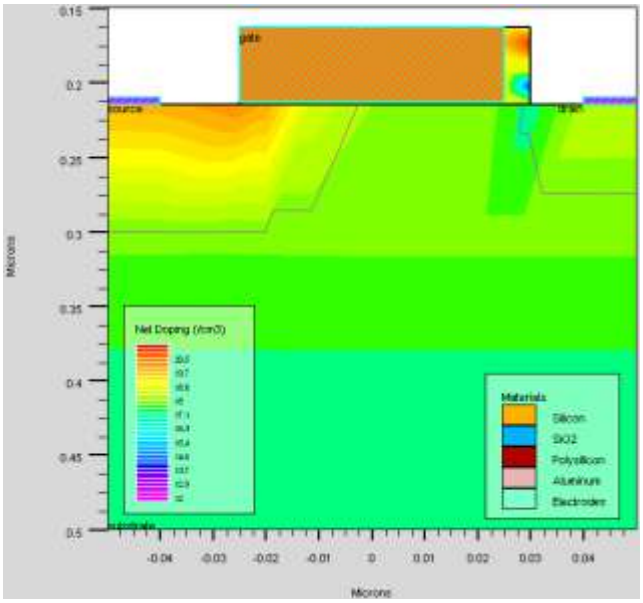

Figure1. Asymmetric MOSFET with LDD at drain only

III. ASSYMMETRIC MOSFET STRUCTURE WITH UNEQUAL JUNCTION DEPTHS

Another asymmetric MOSFET has been designed where the junction depths of source and drain are unequal. The junction depth here of the drain is deeper than that of source. It indicates that the fields kept away from the Si-SiO$_2$ interface, thus protecting it from damage. As junction depth is decreased, parasitic series resistance increases [8]. This MOSFET is designed with the same parameters as the previous one but the

 ISSN: 2321-8169
1129 - 1131

junction depth at the drain is more than that at the source. This is achieved by diffusing lightly doped drain and source regions, and then oxide spacer is formed and then heavy source and drain regions were diffused. Then after, oxide was etched from the part of the drain where extra dose of arsenic was to be added to increase the drain junction depth. For that metal (aluminium) was deposited on the entire n MOS and it was again etched from the drain side, so that while adding more arsenic impurities, it would not penetrate and create disturbance

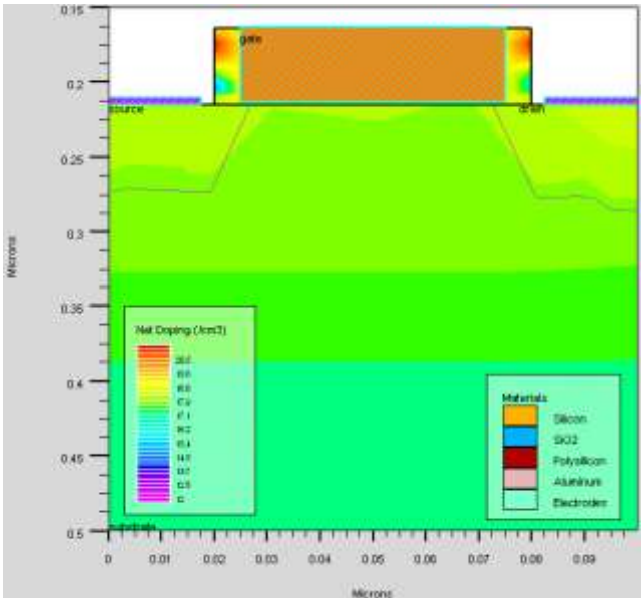

Figure2. Asymmetric MOSFET with unequal junction depths

in other parts of the MOSFET. After adding extra dose of impurity, the junction depth at drain increased. Then the entire metal was etched and proper patterning was done to form the contact terminals as shown in fig. 2.

IV. Simulation Results

Figs. 3 and 4 show the simulation results of the 50nm asymmetric MOSFETs with LDD at drain only and asymmetric MOSFET with unequal junction depths respectively.

In case of asymmetric MOSFET with LDD at drain only, the threshold voltage is 0.15V at V_{DS} =0.05V, the on-current is 1171 µA/µm, off-current is 30 µA/µm and subthreshold swing, SS= 225 mV/dec at VDS=1V. In case of asymmetric MOSFET with unequal junction depths, the threshold voltage is 0.18V at V_{DS} =0.05V, the on-current is 222 µA/µm, off current is 2.35 µA/µm and subthreshold swing, SS= 129mV/dec at V_{DS}=1V. These results are tabulated in table 1.

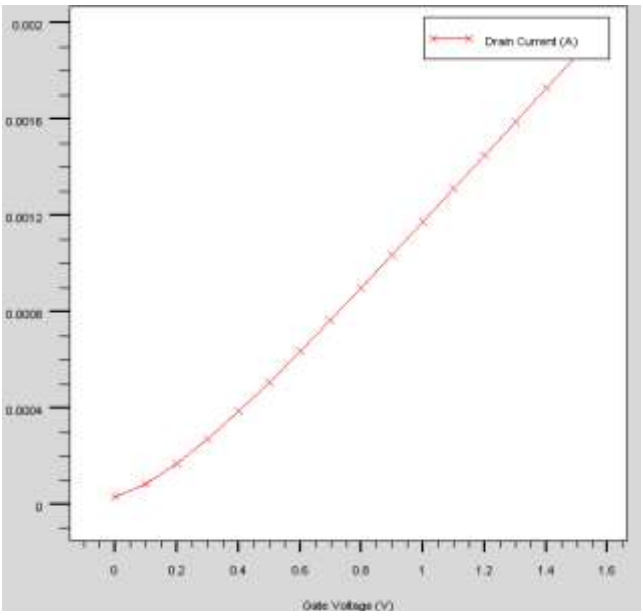

Fig. 3 ID-VG curve of asymmetric MOSFET with LDD at drain only

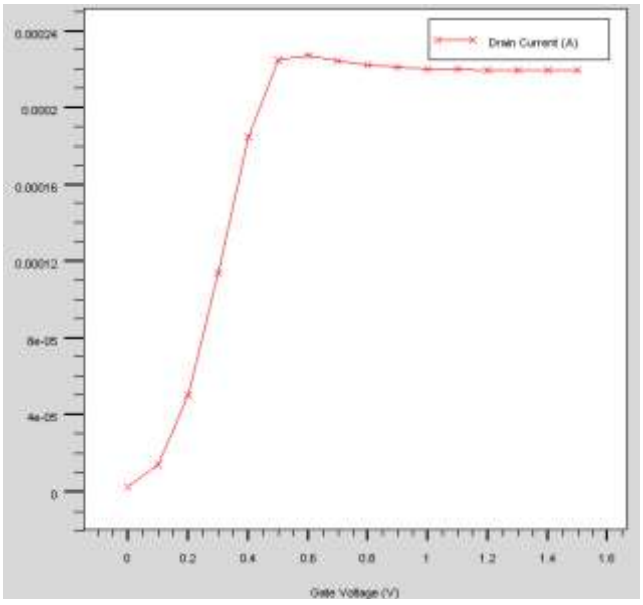

Fig. 4 ID-VG curve of asymmetric MOSFET with unequal junction depths

Light doping leads to increase in the depletion region width as doping is inversely proportional to depletion width, thus decreasing the electric field across the region [10]. This results into decrease in hot carrier effects. The LDD structure thus reduces short channel effects. Also, to minimize short channel effects, we want shallow source and drain regions but the parasitic resistance of these regions will increase when diffusion depth (X_J) is reduced. Lesser doping results in lower peak E-field hence hot-carrier effects are reduced but series resistance increased. Due to the presence of LDD regions, on current is less in symmetric MOSFET.

The asymmetric MOSFET is thus designed with no LDD at the source side. In asymmetric MOSFET with LDD at drain only, parasitic resistance is less and thus on current, I_{ON} is more while that in case of asymmetric MOSFET with unequal junction depths, the diffusion depth at drain is more than that at source. This will keep the electric fields away from the Si-SiO_2 interface and thus prevent it from hot electron effects and impact ionization [11].

V. CONCLUSION

The 50nm gate length MOSFET was thus designed and simulated. Since in symmetric MOSFET there exist parasitic resistances in the LDD region, the on current decreases and hence the switching speed of the transistor reduces. LDD structure reduces the short channel effects, but as MOSFET is further scaled down, it becomes necessary to control the short channel effects for which two asymmetric MOSFET structures where LDD at drain only and unequal junction depths with same gate length were designed. Finally both symmetric and asymmetric structures of 50nm gate length MOSFETs were simulated and a comparative study was done. On comparing the symmetric and asymmetric MOSFETs, a significant increase in the on current was observed.

TABLE I. SIMULATION RESULTS

Parameters	**LDD at drain only**	**Unequal Junction Depths**
V_{TH} (V) @V_{DS}= 0.05V	0.15	0.18
I_{ON} (µA/µm) @VGS=1V and V_{DS}= 1V	1171	222
I_{OFF} (µA/µm) @ V_{GS}=0V and V_{DS}= 1V	30	2.35
SS (mV/dec) @ V_{DS}=1V	225	129

ACKNOWLEDGMENT

I am grateful to my colleagues for their valuable suggestions and my parents for their constant support and understanding.

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