Closed Loop Control of DSMST Converter for Ev Applications

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Abstract—Transformerless step-down and step-up DC-DC topologies are currently extensively employed in a variety of applications. A positive output voltage SEPIC-type DC-DC converter without a transformer is proposed in this article. This configuration has the benefit of input continuous current over the traditional buck-boost converter, making it better suited for use with electric vehicles. Moreover, it has an increase in gain that is quadratic of the voltage gain of a standard topology. Also, the suggested converter has a constant current output, which decreases the output voltage ripple and reduces the current stress on the converter's output capacitor. As a result, this converter can generate an extensive range of voltages with less input and output ripples. In addition, closed loop control of DSMST converter is presented in the paper using PI control Ziegler-Nichols method. In the end, simulation findings are shown to support the converter's closed loop study.

Keywords- DC-DC Converters, SEPIC Converter, Electric vehicle...

1. **INTRODUCTION:**

With increasing global concern for the environment and the need for sustainable transportation solutions, electric vehicles have gained significant traction in recent years. These vehicles, powered by low-carbon electricity and equipped with energy-efficient technology, are considered a key factor in the de-carbonization of transportation and the emergence of lowcarbon cities [1]. To support the growth and success of the electric vehicle industry, technological innovation is crucial [2]. One area of technological innovation that plays a vital role in electric vehicle applications is the development of DC-DC converters. DC-DC converters are essential components for various applications, including renewable energy systems, electric traction, battery charging, and fuel cell energy conversion systems [2, 3]. Among the various DC-DC converter topologies, the SEPIC converter stands out as a versatile solution for electric vehicle applications. The SEPIC converter, short for Single-Ended Primary Inductor Converter, offers many features that make it well-suited for electric vehicle applications. Firstly, SEPIC converters provide a better potential for change while decreasing the potential for output expansion. This means that they can efficiently step up or step down the voltage, allowing for seamless integration with different components in the electric vehicle system. Furthermore, SEPIC converters have been found to have a high gain, making them suitable for applications requiring a significant voltage boost [4-7].

The typical buck-boost network has a modest structure and great efficiency, but it is plagued by discontinuous input current and is restricted in its ability to increase voltage [8 - 10]. But the quadratic buck-boost design lets you change voltages in a lot of different ways without needing a duty cycle that is too high [11]. In reference [12], the quadratic buck-boost converter with a positive output voltage is first talked about. The achievement of this is attained by the implementation of a cascaded configuration including two conventional buck-boost converters. When the duty ratio of the circuit is larger than 0.5, however, this converter will not function correctly because the input voltage is clamped by the diodes to its output value. It is hypothesized in [13] that a quadratic buck-boost configuration with non-inverting output voltage can be created by adding an extra switch to the framework of a regular buck-boost circuit. The converter has a straightforward design, but its input and output currents are unreliable due to their discontinuous nature. It is important to point out that converters with intermittent source current are not appropriate to use in renewable energy sources based applications. Additionally, the current stress raises due to discontinuous output current on the filter capacitor, which in turn makes output voltage ripple worse [14-18]. In the paper [19], a quadratic type buck-boost network with singleswitch is reported. DSMST converter was formed by inserting a switching cell containing one active and one passive switches, one LC network for energy recycle, and altering the output diode with the inductor (see fig. 1). This converter features both continuous, input and output current at all the times. Because of the comparatively high number of elements utilized in this

structure, particularly the number of diodes, the circuit architecture is made more complicated, which results in an increased amount of power loss. In addition, the polarity of the output voltage of this converter is a negative value. The paper [20] presents a quadratic buck-boost converter that has zero output voltage ripple at an operational point that can be chosen by the user. This converter has a positive output voltage and a constant input current, but its topology requires two floating power switches, which drives up the price of the driver circuit for gate pulses.

In this article, a modified SEPIC configuration with a non-inverting output voltage is presented. This converter has various advantages, including the following ones:

- The suggested converter accepts a continuous input current, which considerably eliminates the demand for a filter at the input port and makes it more suitable for the use of nonconventional systems.
- Because the suggested configuration provides a continuous output current, it reduces the amount of current stress placed on the output capacitor, which in turn reduces the amount of output voltage ripple.
- The converter that has been presented is capable of functioning across a broad range of output voltage.

The problem with the common ground has been solved because the proposed converter has a non-inverting (+ve) output voltage.

2. Construction and Operation of Proposed DSMST Converter

The proposed SEPIC converter which is shown in Fig. 1. It includes three inductors Lin, LSC, and Lout, three capacitors C_{SC} , C, and C_{out} , two switches S_{SC} & S, and two diodes D_{SC} and D. The DSMST configuration is based on the classic SEPIC converter, but with the addition of a switching cell. In addition, for the continuous output current, the output diode and inductors are switched. Because the proposed converter's switches function synchronously, a single pulse is required to regulate the configuration.

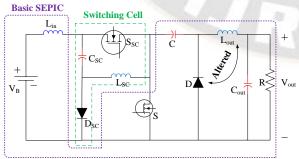


Fig. 1. Circuit diagram of proposed DSMST converter

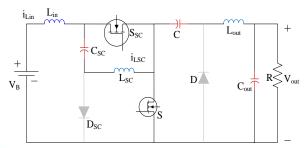


Fig. 2. ON state circuit diagram of proposed converter. To facilitate the analysis, the following assumptions are taken into consideration:

- All the components, including switches and diodes, are assumed to be lossless.
- The voltage stress of capacitors is expected to be stable.
- In continuous condition mode (CMM), the steady-state analysis is done.

'ON state':

In this state, the active switches S_{SC} and S are triggered with a pulse simultaneously although the passive switches D_{SC} and D are turned OFF because of the reverse-biased condition. The inductors L_{in} , L_{SC} and L_{out} are energized by the DC input supply, capacitor C_{SC} and capacitor C, respectively. Therefore, capacitor C_{SC} and C are discharged as shown in Fig. 2. This mode's differential equations can be written as

The second section of the second section is shown as
$$L_{in} \frac{diL_{1}}{dt} = v_{in}$$

$$L_{sc} \frac{diL_{sc}}{dt} = v_{csc}$$

$$L_{out} \frac{diL_{out}}{dt} = v_{c} - v_{out}$$

$$C_{sc} \frac{dvC_{sc}}{dt} = -iL_{sc}$$

$$C \frac{dvC}{dt} = -iL_{out}$$

$$C_{out} \frac{dvC_{out}}{dt} = iL_{out} - \frac{v_{0}}{R}$$

$$C_{out} \frac{dvC_{out}}{dt} = iL_{out} - \frac{v_{0}}{R}$$

$$C_{out} \frac{dvC_{out}}{dt} = iL_{out} - \frac{v_{0}}{R}$$

Fig. 3. OFF state circuit diagram of proposed converter

'OFF' state: In this period, the active switches S_{SC} and S are simultaneously turned OFF besides the passive switches D_{SC} and D are turned ON. The capacitor C_{SC} is energized by inductor L_{in} , and the capacitor C is energized by inductor L_{SC} .

Furthermore, the L_{out} inductor energizes the C_{out} capacitor as shown in Fig. 3. This mode's differential equations can be written as

$$L_{in} \frac{diL_{in}}{dt} = v_{in} - v_{c_{sc}}$$

$$L_{sc} \frac{diL_{sc}}{dt} = -V_{C_{sc}}$$

$$L_{3} \frac{diL_{3}}{dt} = -v_{out}$$

$$C_{sc} \frac{dvC_{sc}}{dt} = iL_{sc}$$

$$C_{sc} \frac{dvC_{sc}}{dt} = iL_{sc}$$

$$C_{out} \frac{dvC_{out}}{dt} = iL_{out} \frac{v_{out}}{R}$$
(2)

The voltage across the capacitors C_{sc} and C, as well as the output capacitor, may be easily computed by applying the volt-second balancing principle to the inductors L_{in} , L_{sc} , and

$$V_{C_{SC}} = \frac{1}{1 - D} V_{in}$$

$$V_{C} = \frac{D}{(1 - D)^{2}} V_{in}$$

$$V_{out} = (\frac{D}{1 - D})^{2} V_{in}$$
 (3)

3. Considerations of two switch buck-boost converter topology:

To ensure the successful functioning of the converter, it is imperative that the components are designed in a suitable manner. Moreover, it is important to note that the operation of the converter in Discontinuous Conduction Mode (DCM) presents certain drawbacks, including a sluggish dynamic response that is contingent upon factors such as switching frequency, output power, and inductor values. Additionally, the semiconductors in the system experience high levels of current and voltage stress. Therefore, it is recommended that the proposed converter be designed to operate under Continuous Conduction Mode (CCM) conditions. Hence, the primary equations for designing the DSMST converter in Continuous Conduction Mode (CCM) operation are hereby presented and substantiated through the simulation outcomes.

3.1 Selection of Duty Cycle: -

As a result, the DSMST converter's voltage gain may be calculated as follows:

$$M(D) = \frac{V_0}{V_{in}} = (\frac{D}{1 - D})^2$$
 (4)

It stands out that the presented converter's voltage conversion ratio is square compared to that of the typical buck-boost circuit. Therefore, the DSMST configuration operates in a larger range of output voltage than a traditional buck-boost circuit. The DSMST converter operates in step-down mode when the duty cycle of switches is below 0.5, and in step-up mode when the duty cycle is equal to or greater than 0.5. The average current in

the inductors may be calculated by using the ampere-second balancing theory on the capacitors C_{SC} , C, and C_{out} .

$$I_{L_{in}} = \left(\frac{D}{1-D}\right)^2 \frac{V_{out}}{R}$$

$$I_{L_{sc}} = \frac{D}{1-D} \frac{V_{out}}{R}$$

$$I_{L_{out}} = \frac{V_{out}}{R}$$
 (5)

3.2 Voltage stresses on active & passive switches: -

The voltage stresses on the diodes could exist by calculating with Mode 1 as follows:

$$V_{DSC} = \frac{1}{1 - D} V_{in}$$

$$V_{D} = \frac{D}{(1 - D)^{2}} V_{in}$$
 (6)

Moreover, from Mode 2 the voltage stresses on the active switches will be determined as:

$$V_{SC} = \frac{1}{(1-D)^2} V_{in}$$

$$V_S = \frac{D}{(1-D)^2} V_{in} \quad (7)$$

3.3 Current stresses on active & passive switches: -

The switching current stresses on S_{SC} and S will be determined from

$$I_{SC} = D(I_{Lin} + I_{LSC}) = (\frac{D}{1 - D})^2 \frac{V_{out}}{R}$$

$$I_S = D(I_{Lout} - I_{Lin}) = \frac{D(1 - 2D)}{(1 - D)^2} \frac{V_{out}}{R}$$
(8)

The diodes current stresses on D_{DSC} and D are attained as:

$$I_{DSC} = (1 - D)(I_{Lin} + I_{LSC}) = (\frac{D}{1 - D})\frac{V_{out}}{R}$$

$$I_D = (1 - D)(I_{LSC} + I_{Lout}) = \frac{V_{out}}{R}$$
(9)

3.4 Ripple current on the inductors: -

The ripple current on the inductors is from mode-1 can be expressed as,

$$\Delta I_{Lin} = \frac{V_{Lin}}{L_{in}} DT_s = \frac{DV_{in}}{L_{in}f_s}$$

$$\Delta I_{LSC} = \frac{V_{LSC}}{L_{SC}} DT_s = \frac{DV_{in}}{(1 - D)L_{SC}f_s}$$

$$\Delta I_{Lout} = \frac{V_{Lout}}{L_{out}} DT_s = \frac{D^2V_{in}}{(1 - D)L_{out}f_s}$$
(10)

The active switches controlled switching frequency (fs) needs to be considered. To confirm that the total inductors function in Continuous Conduction Mode (CCM),

$$L_{in} > \frac{(1-D)^4 R}{2D^3 f_s}$$

$$L_{SC} > \frac{(1-D)^2 R}{2D^2 f_s}$$

$$L_{out} > \frac{(1-D)R}{2f_s}$$
(11)

Or else, the circuit will start performing under discontinuous current mode (DCM).

3.5 Capacitors voltage ripple: -

The DSMST converter capacitors voltage ripple will be computed by:

$$\Delta V_{CSC} = \frac{\Delta Q_{CSC}}{C_{SC}} = \frac{D^2 V_{out}}{(1 - D)RC_{SC}f_s}$$

$$\Delta V_C = \frac{\Delta Q_C}{C} = \frac{DV_{out}}{RCf_s}$$

$$\Delta V_0 = \frac{\Delta Q_{Cout}}{C_{out}} = \frac{(1 - D)V_{out}}{8L_{out}C_{out}f_s^2}$$
(12)

The relevant capacitors can be preferred based on D, Fs, V_{out} , R, and the permitted voltage ripple.

3.6 Efficiency analysis: -

In order to streamline the analysis of efficiency, the impact of voltage ripple in capacitors and current ripple in inductors is disregarded. Consequently, the total power losses of switch S_{sc} can be determined.

$$P_{sw}(S_{sc}) = P_{rDSsc} + P_{sw,off(Ssc)}$$

$$= r_{DSsc} I_{Ssc,rms}^2 + \frac{1}{2} I_{Ssc} V_{Ssc} t_{off1} f_s$$

$$= r_{DSsc} \frac{D^3}{(1-D)^4} \frac{P_0}{R} + \frac{1}{2} \frac{P_0}{(1-D)} t_{off1} f_s \quad (13)$$

Where t_{off1} and r_{DSsc} are the switch S_{sc} 's turn-on delay time and turn-off resistance, respectively. The switch S's overall losses in step-down mode are.

$$P_{SW}(S, step - down) = P_{rDS} + P_{SW,off(S)}$$

$$= r_{DS}I_S^2, rms + \frac{1}{2}I_SV_St_{off2}f_S$$

$$= r_{DS}\frac{D(1-2D)^2}{(1-D)^4}\frac{P_0}{R} + \frac{1}{2}\frac{(1-2D)P_0}{(1-D)^2}t_{off2}f_S$$
 (14)

Where t_{off1} and r_{DS1} are turnoff delay time and on-resistance of the switch S_{sc} , respectively. The total loss of active device S, in step-up condition is

$$P_{SW(S,step-up)} = r_{DS}I_{S,rms}^2 + V_{FDS}I_S$$

$$= r_{DS}\frac{D(1-2D)^2}{(1-D)^4}\frac{P_0}{R} + V_{FDS}\frac{D(1-2D)}{(1-D)^2}\frac{V_{out}}{R}$$
(15)

Where V_{FDS2} and V_{FD2} are body diode threshold voltages for the switch S_2 respectively. For the diodes D_1 and D_2 the forward voltage losses are obtained as:

$$P_{DVF} = V_{FDSC}I_{DSC} + V_{FD}I_{D}$$

$$= V_{FDSC}\frac{DV_{out}}{(1-D)R} + V_{FD}\frac{V_{out}}{R}$$
(16)

Where V_{FD1} and V_{FD2} are D_1 and D_2 , diodes threshold voltages correspondingly. The derivation of inductor losses is as follows:

$$P_{L} = r_{Lin}I_{Lin,rms}^{2} + r_{Lsc}I_{Lsc,rms}^{2} + r_{Lout}I_{Lout,rms}^{2}$$

$$= r_{Lin}\frac{D^{4}P_{0}}{(1-D)^{4}R} + r_{Lsc}\frac{D^{2}P_{0}}{(1-D)^{2}R} + r_{Lout}\frac{p_{0}}{R}$$
(17)

Where r_{L1} , r_{L2} , and r_{L3} are, respectively, L_1 , L_2 , and L_3 's equivalent series resistances (ESR). In step-down and step-up

states, the DSMST circuit efficiency will be expressed as follows:

$$= \frac{P_0}{P_0 + P_{SW(S_1)} + P_{SW(S_2,step-down)} + P_{DVF} + P_L}$$
(18)
$$= \frac{\eta_{step-up}}{P_0} = \frac{P_0}{P_0 + P_{SW(S_1)} + P_{SW(S_2,step-up)} + P_{DVF} + P_L}$$
(19)

4. Closed Loop Control of DSMST Converter :-

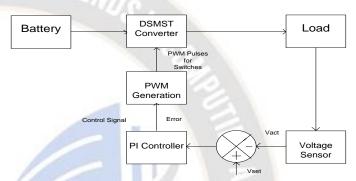


Fig.4 Closed loop block diagram of DSMST converter

5. The Ziegler-Nichols method of PI Tuning:

The Ziegler-Nichols method is a well-known heuristic technique for tuning PID controllers, and it is widely used in the field of control systems. Here are some key points about the Ziegler-Nichols method:

The Ziegler-Nichols method is a heuristic method of tuning a PID controller, developed by John G. Ziegler and Nathaniel B. Nichols. It involves setting the integral and derivative gains to zero and then gradually increasing the proportional gain until the system oscillates at a constant amplitude. The critical gain and critical period of oscillation are then used to calculate the controller parameters. The method provides a simple approach to tuning PID controllers and can be used for systems with feedback. It is known for its ability to generate aggressive gain and overshoot, which is suitable for applications requiring best disturbance rejection.

Table 1. Ziegler-Nichols Tuning Rule table based on Critical Gain and Critical Period

una Critical I crioa					
Type of Controller	Кр	Ti	Td		
P	0.5 kcr	ω	0		
PI	0.45 ker	0.84 Pcr	0		
PID	0.6 kcr	0.5 Pcr	0.125 Pcr		

Where KP = Proportional Gain, Ti = Integral Time, Td = Derivative Time Kcr = Critical Gain and Pcr = Critical Period

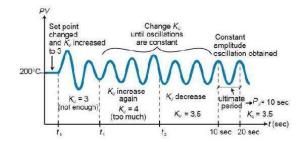


Fig. 5. Graphical Presentation for P, I, and D Gains According to the Ziegler–Nichols

Table 2. The parameters of the DSMST converter are as follows:

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S.No	Components	Notation	Values
1	Input Voltage	V _{in}	12V
2	Output Voltage	V _o	100V
3	Switching Frequency	f _s	80KHz
4	Output Load	R _o	2.8571 Ω
5	Output Power	P _o	3.5Kw
6	Duty cycle	D	0.7427 or 74.27%
7	Inductor 1	L _{in}	111.4μΗ
8	Inductor 2	L _{SC}	433μΗ
9	Inductor 3	L _{out}	321.57μΗ
10	Capacitor 1	C _{SC}	187.59μF
11	Capacitor 2	С	64.98μF
12	Capacitor 3	C_{out}	1.56μF
13	Inductor Ripple Current 1	ΔI_{Lin}	1A
14	Inductor Ripple Current 2	ΔI_{LSC}	1A
15	Inductor Ripple Current 3	ΔI_{Lout}	1A
16	Capacitor Ripple Voltage 1	ΔV_{CSC}	5V
17	Capacitor Ripple Voltage 2	ΔV_C	5V
18	Capacitor Ripple Voltage 3	ΔV_{Cout}	1V
19	M(D)	$\left(\frac{D}{1-D}\right)^2$	8.334

6. Simulation Results

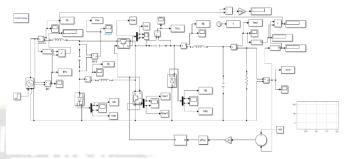


Fig.6. Simulink diagram for closed loop of DSMST converter 1) The Fig. 6 shows the Simulink diagram of closed loop dc dc converter which has all the with respect to the MATLAB software such as inductors, capacitors, diodes, voltmeters, ammeters, scopes for viewing results, workspace blocks which are used to carry the obtained result or output the workspace of command window so that results can be extracted there, displays, summer, step input signal etc,...

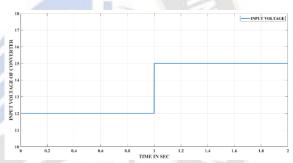


Fig.7. Simulated waveform of Input Voltage.

The above Fig.7 represents the simulted waveform of Voltage across Input side. In the figure the Y-axis demonstrates Input Voltage across DSMST converter where X-axis as time in seconds.

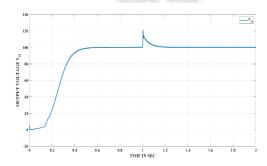


Fig. 8. Simulated waveform of Output Voltage V_0 .

Output voltage across the load is shows in Fig. 8. The Y-axis of the waveform represents the switched output voltage, while the X-axis represented the time (in seconds). The Y-axis values range from 0 to 140, while the X-axis values range from 0 to 2.

The below Fig.9 illustrates waveform of switched cell switch voltage which is simulated by using time in seconds

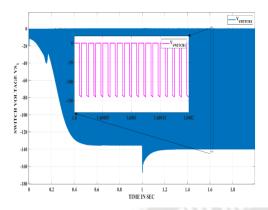


Fig 9. Simulated waveforms of Switched Cell Switch Voltage. In the above waveform Switched cell switch voltage represents upon Y-axis ranges from 0 to --180 whereas Time in seconds represents on X-axis ranges from 0 to 2.

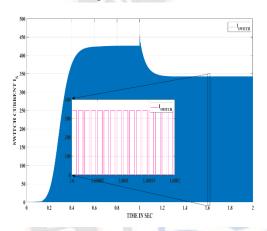


Fig.10. Simulated waveforms of Switched Cell Switch Current. The above Fig.10 represents the simulated waveform between switched cell switch current and time in seconds . Switched cell switch current as Y-axis taken range from 0 to 500 where on X-axis taken range from 0 to 2

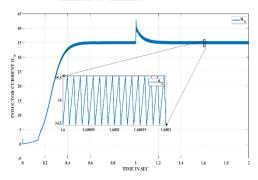


Fig.11. Simulated waveforms of output Inductor current The above Fig.11 is a simulated waveform plotted between output Inductor current vs Time(sec). output Inductor current presented on Y-axis and Time on X-axis. Therefore , Y-axis ranges from -5 to 45 where X-axis from 0 to 2.

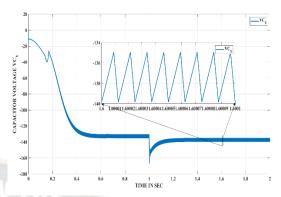


Fig.12. Simulated waveforms of Switched capacitor voltage.

The above Fig.12. illustrates waveform of Switched capacitor voltage which is simulated by using time in seconds. In the above waveform Switched capacitor voltage represents upon Y-axis ranges from 0 to -180 whereas Time in seconds

represents on X-axis ranges from 0 to 2.

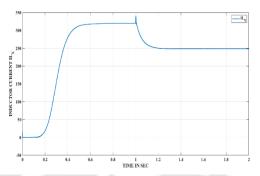


Fig.13. Simulated waveforms of Input inductor current.

The above Fig.13 represents the simulated waveform of Input inductor current to Time in seconds. In the figure the Y-axis demonstrates of Input inductor current where X-axis as time in seconds. The values of Y-axis range taken from -50 to 350 where X-axis range from 0 to 2.

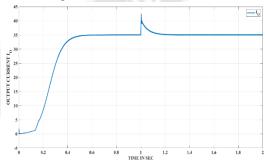


Fig.14. Simulated waveforms of Output Current I_0 . The output current which is simulated shows in Fig. 14. The Y-axis of the waveform represents the output current, while the X-axis represented the time (in seconds). The Y-axis values range from 0 to 45, while the X-axis values range from 0 to 2.

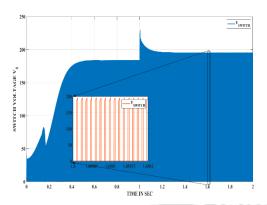


Fig.15. Simulated waveform of switch voltage.

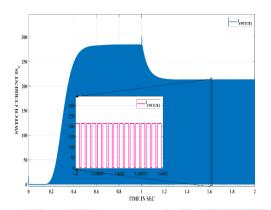


Fig.16. Simulated waveform of Switch current

In the above Fig.16 we can observe the simulated waveform between Switch current and Time(sec). Therefore from the simulted waveform plotting we get Ripple current.

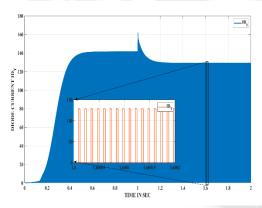


Fig.17. Simulated waveform of Output Diode current...

The above Fig.17. illustrates waveform of Output Diode current which is simulated by using time in seconds. In the above waveform of Output Diode voltage represents upon Y-axis ranges from 0 to -180 whereas Time in seconds represents on X-axis ranges from 0 to 2.

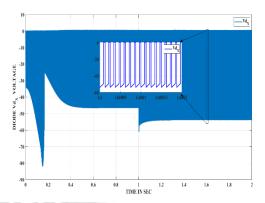


Fig.18. Simulated waveform of Output Diode voltage.

The above Fig.18 is a simulated waveform plotted between Switched Cell Diode voltage and Time(sec). Switched Cell Diode current presented on Y-axis and Time on X-axis. Therefore, Y-axis ranges from 0 to -80 where X-axis from 0 to 2.

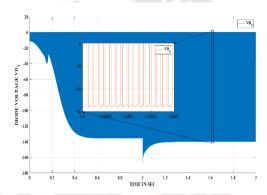


Fig.19. Simulated waveform of Diode Voltage.

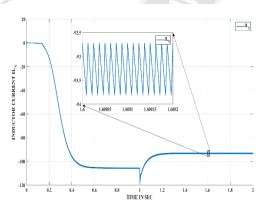


Fig.20. Simulated waveform of inductor current.

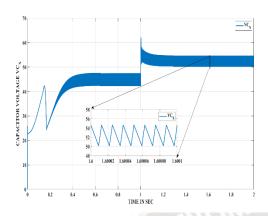


Fig.21. Simulated waveforms of capacitor voltage Vc.

The above Fig.21, waveform of capacitor voltage which is simulated by using time in seconds. In the above waveform Switched capacitor voltage represents upon Y-axis ranges from 0 to 70 whereas Time in seconds represents on X-axis ranges from 0 to 2.

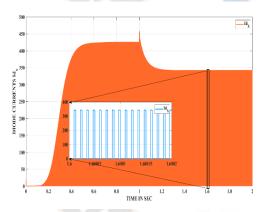


Fig.22. Simulated waveform of inductor current.

The output current which is simulated shows in Fig. 22. The Y-axis of the waveform represents the inductor current, while the X-axis represented the time (in seconds). The Y-axis values range from 0 to 500, while the X-axis values range from 0 to 2.

7. CONCLUSION

In this work, a modified SEPIC called DSMST configuration is shown. The CCM circuit operation demonstrates the fundamental operation and steady-state analysis of the proposed topology. In addition, closed loop control using Ziegler Nichols method which has shown that the performance has been improved and the output voltage reached 100 v and MATLAB simulation validates the incorporation of this approach to small signal analysis. The performance of the suggested converter is validated by simulation data, The suggested converter has various advantages, including constant input and output currents. As a result, the input and output filters can be made smaller. The given converter features a quadratic voltage gain

and a positive output voltage polarity. Hence, the given configuration is a promising topology for EV systems.

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